MARKED-UP VERSION SHOWING CHANGES

Method For Determining Failure Rate And Selecting Best Burn-In time

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention pertains to methods for determining failure rate and selecting best burn-in time~~,—and~~ which can ~~have particular application to~~ provide both error range and risk estimation by numerical approach.

2. Description of the Prior Art

~~Accompany with increasing~~ As the complexity of integrated circuits and ~~increasing~~ the difficulties of market contest increase, quality and reliability of produced integrated circuits ~~is~~ have became more important than ever. Therefore, how to control the qualities of produced integrated circuits, how to estimate failing risk of integrated circuits while they are used by end-users, and how to balance production cost and quality promise are some important ~~challenge of~~ challenges for the quality department of integrated circuits manufacturers.

In general, the relation between failure rate of integrated circuits and time, both for testing and for application of end-users, is usually ~~is~~ called a bathtub curve. As shown in FIG. 1, ~~accompanying~~

with the increase of time (period), the bathtub curve can be divided into infant mortality period, normal life period and wear out period. Whereby, infant mortality period usually corresponds to failure induced by defects of fabrication, and usually lasts about several weeks; normal life period usually corresponds to some random failures, and usually lasts about twenty years, thirty years or more; wear out period usually corresponds to failure induced by long-time waste, and is continuously increased while time goes by.

Because most of integrated circuits will have been replaced with new designs and new technologies before the wear out period is reached, ~~manufactories~~ manufacturer usually only need to test all produced integrated circuits through the infant mortality period to select all ~~failing~~ integrated ~~circuits that~~ circuit failures induced by imperfect fabrication. Thus, all tested integrated circuits are suitable for selling, and the only risk is some random failures. Moreover, elimination of these random failures and prolongation of normal life-time only can be achieved by improvements of fabrication of integrated circuits, ~~but~~ can not be achieved ~~only~~ by operation of quality department.

However, owing to limitation of time, it is impossible for the quality department to test all produced integrated circuits through both the infant mortality period and the normal life period, even only through the infant mortality period. As usual, the quality department only performs a stress test~~,~~ or ~~called as~~ an accelerated test~~,~~ to test produced integrated circuits through a specific period under a testing environment ~~in~~ which is more harmful and danger for tested integrated

circuits, and then the relation between the failure rate and testing time is measured. ~~Then, in accordance with the~~ The difference between ~~the difference between~~ the testing environment and a normal operating environment is used to estimate the relation between failure rate and real time, ~~in~~ which is the experienced time under the normal environment.

Indisputably, how to properly and correctly transform the failure rate versus testing time relation into the failure rate versus real time relation, is the key about whether failure rate versus time relation can be properly ~~consulted~~ acquired by the stress test.

Moreover, almost all well-known arts use mathematical formula to estimate the failure rate relation by some tested datas. For example, the popular mathematical formula is the chi square distribution : ~~$\lambda = \chi^2(2(r+1) \cdot B)/2t$~~ $\lambda = \chi^2[2(r+1)B]/2t$. Herein, λ is the failure rate, χ is the chi square function, r is failing number, B is confidence and t is time, and value of χ is consulted from a pre-established table.

Significantly, because the failure rate versus time relation is ~~consulted~~ acquired by referring to the formula in accordance with testing records, well-known arts ~~can not avoid~~ have the following disadvantages: (1) the difference between the experimental value and the theoretical value can not be found by the used formula; (2) the best burn-in time only can be ~~consulted~~ acquired by experience or formula, it can not be ~~consulted~~ acquired by the relation between the best burn-in time and the corresponding risk; (3) the reliability of produced

integrated circuits can not be ~~promised~~ assured by ensuring the estimated value which is almost the best value in accordance with the comparison between the experimental value and the theoretical value.

As a short summary, it is obviously that conventional arts can not efficiently determine the failure rate versus time relation and select the best burn-in time. Thus, it is necessary to develop a new method to analysis the testing records of the stress test and to effectively improve efficiency of quality department.

SUMMARY OF THE INVENTION

Objects of the present invention at least include providing a numerical method for providing both error range and risk estimation.

Objects of the present invention further comprise providing a method for controlling qualities of produced integrated circuits, estimating failing risk of users of produced integrated circuits, and balancing requirements of both production cost and quality promise.

On the whole, one method ~~present~~ provided by the invention at least includes following basic steps: ~~Method for determining failure rate and selecting a best burn-in time, comprising:~~ ~~provide~~ providing numerous integrate circuits; ~~performs~~ performing a life-time testing process, wherein a failure rate versus testing time relation is established by measuring the life-time of each integrated circuit under a testing environment, ~~wherein~~ an acceleration factor function also is established under the testing environment, and the acceleration factor

function is related to the relationship between a testing time of the testing environment and a real time of a normal operating environment; ~~performs~~ performing a simulating process that a testing time function ~~is used~~ to simulate the failure rate versus testing time relation; ~~performs~~ performing a transforming process by using the acceleration factor function to transform the testing time function into a real time function, wherein a knee point of the real time function corresponds to an operation time which is the best burn-in time; and ~~performs~~ performing an integrating process to integrate the real time function through a calculating region to ~~consult~~ acquire an accumulated failure rate versus real time function, wherein the calculating region is a region in which the real time is larger than the best burn-in time.

Besides, ~~the invention further comprises that~~ while more than one integrated circuits are failed before the knee point, the method further ~~comprising~~ comprises deleting part of testing records and re-calculating the best burn-in time until only one integrated circuit is ~~fail~~ failed before the knee point.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

FIG. 1 is a brief illustration of the well-known relationship between failure rate and time for integrated circuits;

FIG. 2 is a brief flow chart of one preferred embodiment of

this invention;

FIG. 3 is a brief flow chart of another preferred embodiments of this invention; and

FIG. 4A through FIG. 4C are some referring figures for showing how to decide and find required knee point.

DESCRIPTION OF THE PREFERRED EMBODIMENT

This disclosure of the invention is submitted in furtherance of the constitutional purpose of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

One major disadvantage of conventional arts is that ~~values of part used~~ parameters and ~~values of part used~~ functions~~,~~ such as chi square function~~,~~ are ~~consulted~~ acquired from some pre-established tables, ~~especially~~ and the same pre-determined tables ~~are~~ is used to analysis different testing records of different samples. It is indisputable that some external variables, which are not ~~consulted~~ acquired from testing records, are used to calculate the failure rate versus time relation, and then the failure rate versus time relation can not be obtained only by testing records. ~~Aims on previous discussion, the~~ The claimed invention presents a way to estimate the failure rate versus time relation only in accordance with testing records, and then only errors induced by estimating process will be an issue but errors induced by external variables will not be an issue.

One preferred embodiment ~~is~~ includes a method for

determining failure rate and selecting a best burn-in time. As shown in FIG. 2 ~~shows~~, the embodiment comprises the following essential steps:

As shown in preparing block 21 ~~shows~~, ~~provides~~ numerous integrate circuits are provided. Whereby, each integrated circuit is similar to other integrated circuits except unavoidable tolerance of fabricating process.

~~As shown in life-time~~ Life-time testing block 22 ~~shows,~~ performs a life-time testing process to establish ~~a~~ an experimental failure rate versus testing time relation by measuring the life-time or failure rate of each said integrated circuit under a testing environment which is well-known as a bathtub experiment having a curve of experiment data with the shape similar to FIG. 1. The bathtub curve can be divided into infant mortality period, normal life period and wear out period. Moreover, an acceleration factor function or an acceleration coefficient function of the bathtub experiment also is established under the testing environment. ~~Herein, the acceleration factor function is related to the relationship between a testing time of the testing environment and a real time of the normal operating environment.~~ Moreover, the testing environment is adjusted to let (failure rate)/(unit time) in the testing environment ~~is~~ larger than the (failure rate)/(unit time) in a normal operating environment, and in general it is achieved by increasing working voltage of integrated circuits, increasing temperature, increasing pressure or other ways. Obviously, contents of the acceleration factor function ~~is~~ are decided by the difference between the testing environment and the normal operating environment, and the acceleration factor function could be a constant,

a linear function or a nonlinear function. Further, as discussed above, the failure rate versus testing time relation can be divided into three periods in according to value of the testing time, the three periods are ~~a~~ an infant mortality period, a normal life period and a wear out period.

As shown in simulating block 23 ~~shows~~, ~~performs~~ a simulating process that uses a ~~testing time~~ test life function for curve fitting is performed to simulate the experimental failure rate versus testing time relation. Whereby, the simulating process is adjusted to let ~~an error~~ a difference, such as ~~last square error~~ least squares, between the experimental failure rate versus testing time relation and the simulated failure rate versus testing time function is minimized. ~~Further, the testing time function is a function of testing time~~. Moreover, because usually only the infant mortality period and the normal life period must be considered, and also owing to the hint of FIG. 1, the ~~testing time~~ test life function for curve fitting usually is an exponent function, ~~a~~ an ~~polynomial~~ equation of failure rate and testing time or $y=at^b$, wherein a and b are two ~~variable~~parameters, y is the failure rate and t is the testing time. The parameters a and b can be obtained from the substitution of experimental data of failure rate and testing time for y and t. The simulated failure rate versus testing time function $y=at^b$ is then obtained, wherein parameters a and b are obtained from the experimental data of failure rate and testing time.

As shown in transforming block 24 ~~shows~~, ~~performs~~ a transforming process that uses the acceleration factor function is performed to transform the simulated failure rate versus testing time function into a real failure rate versus operation time function.

Whereby the knee point of the real failure rate versus operation time function corresponds to an operation time which is the best burn-in time. ~~By referring~~ Referring to FIG. 1, it is reasonable that while the difference between the simulated failure rate versus testing time function and the real failure rate versus operation time relation is properly minimized by the simulating process, the knee point should corresponds to the end of the infant mortality period and also corresponds to beginning of the normal life period.

As shown in integrating block 25 ~~shows~~, ~~performs~~ an integrating process that integrates the real failure rate versus operation time function through a calculating region is performed to ~~consult~~ acquire obtain ~~an accumulated failure rate real time function~~ a yield ratio ~~(~~ (normal chip number~~)~~) equal to the area under the curve of the real failure rate versus operation time function. Whereby, the calculating region is a region in which the real time is larger than the best burn-in time. Certainly, because integrated circuits usually are not ~~never are used~~ operated ~~to~~ in the wear out period, it is reasonable that integrating process ~~is stopped~~ ends ~~while said testing time in which is corresponds by~~ when said testing time ~~is located in~~ reaches said wear out period, and then result of the integrating process is the accumulated failure rate during the normal life period.

~~Another embodiment of the invention also is a method for determining failure rate and selecting best burn in time. As FIG. 3 shows, the embodiment comprises following essential steps:~~

~~As preparing block 31 shows, provides numerous integrate~~

~~circuits.~~

~~As life-time testing block 32 shows, performs a life-time testing process to establish a failure rate testing time relation by measuring the life-time of each said integrated circuit under a testing environment. Moreover, an acceleration factor function also is established under the testing environment. Herein, the acceleration factor function is related to the relationship between a testing time of the testing environment and a real time of the normal operating environment.~~

~~As transforming block 33 shows, performing a transforming process by using the acceleration factor function to transform the failure rate testing time function into a failure rate real time function.~~

~~As simulating block 34 shows, performing a simulating process that uses a real time function to simulate the failure rate real time relation. Whereby, a knee point of the real time function corresponds to an operation time which is a best burn in time for testing these integrated circuits.~~

~~As integrating block 35 shows, performing an integrating process by integrating the real time function through a calculating region to acquire an accumulated failure rate real time function. Whereby the calculating region is a region in which real time is larger than the best burn in time~~.

~~Indisputably, while the acceleration factor function is a~~

~~constant, the result of performing the simulating process under the testing time is similar to the result of performing the simulating process under the real time, the only difference is the effect of constant. However, while the acceleration factor function is a linear function or a non-linear function, owing to the transformation between the real time and the testing time is not multiplied by a constant or divided by a constant, the knee point of the testing time function usually is different from the knee point of the real time function. In other words, previous embodiments are equivalent while the acceleration factor function is a constant and are not equivalent while the acceleration factor function is not a constant. Moreover, while the acceleration factor function is not a constant, when to perform the simulating process should be decided by the practical effect of the claimed invention. Furthermore, the simulating process can be performed at any time while the acceleration factor function only is a constant; but the timing for performing the simulating process should be decided by both the accumulated failure rate real time function time and the best burn in time while the acceleration factor function is not a single constant~~

Obviously, because the claimed invention never uses any mathematical formula ~~also~~ and never uses any external parameter which is not ~~consulted~~ acquired from the testing records, and also because the claimed invention is a numerical approach method, it is reasonable that the claimed invention can decide the error range by ~~"try and error"~~ trial and approach and also can decide the precision of the ~~consulted~~ acquired ~~accumulated~~ real failure rate versus ~~real~~ operation time function.

Besides, because calculation and application of the knee point is a key point of the claimed invention, and because precision of knee point is directly proportional to cost of the claimed invention. Calculation is further discussed in following paragraphs.

First, the failure rate versus testing time relation is combined by numerous testing records, the failure rate versus real time relation also is combined by these testing records, and the only differences ~~are~~ is ~~only~~ the acceleration factor function.

Next, while more than one integrated circuits ~~are failed~~ fail before a specific testing time in which is corresponding to the knee point, it usually is necessary to perform an ~~optimizating~~ optimization process that deletes part of testing records and performs corresponding processes. While only one integrated circuit ~~is failed~~ fails before a specific testing time ~~in which is corresponding to~~ reaches the knee point, the specific testing time is a best testing time of these integrated circuits.

For example, ~~while~~ the curve of the failure rate versus testing time relation ~~is~~ as shown in FIG. 4A ~~that the curve~~ is formed by the following testing records 6H-12H-18H ...and so on, and it is obviously that ~~12H,~~ the second testing record, 12H is a good knee point and no other obvious knee point is existent, and then the required time function can be ~~consulted~~ acquired from the following testing records 6H-12H-23H ...and so on. However, while the curve of the failure rate versus test time relation ~~is~~ as shown in FIG. 4B ~~that the curve~~ is formed by 6H-12H-18H-24H(knee point)-30H... and so on, or while the

curve of the failure rate versus testing time relation ~~is~~ as shown in FIG. 4C ~~that curve~~ is formed by 6H-12H-18H(near knee point)-24H(near knee point)-30H...and so on, it is necessary to delete the first few testing records~~,~~. ~~for~~ For example, ~~deleting the~~ 6H and 12H are deleted for the curve of FIG. 4C and ~~deleting~~ 6H is deleted for the curve of ~~FIG. 4D~~ FIG. 4B, to let the knee point is the second used testing recorded. And then the time function is calculated while the knee point is properly selected.

Without any question, while it is necessary to decrease the total failure probability that the integrated circuit is used by an end-used during the normal life period, and while at least one testing record is existent after the knee point, it is useful to move the knee backward to prolong the best burn-in time and decrease the normal life period. Moreover, while advantages of both prolonged best burn-in time and decreased failure probability can not cancel the disadvantages of both increased production cost and quality controlling cost, the claimed invention also provides some trustable information to notice both the produce line and the customers that failure probability only can be decreased by improvement of fabrication.

Besides, while these is no enough testing records to ensure the precision of the knee point, the claimed invention can be further expanded to test same integrated circuits several times and find the best knee point by all testing records of all tests.

Although specific embodiments have been illustrated and described, it will be obvious to those skilled in the art that various

modifications may be made without departing from what is intended to be limited solely by the appended claims.

ABSTRACT OF THE INVENTION

~~Method~~ A method for determining failure rate and selecting a best burn-in time~~, comprising:~~ is disclosed. The method comprises the following steps. First of all, ~~provide~~ ~~numerous~~ integrate circuits are provided~~;~~. ~~performs~~ Then a life-time testing process is performed, wherein a failure rate versus testing time relation is established by measuring the life-time of each integrated circuit under a testing environment, wherein an acceleration factor function also is established under the testing environment~~, the acceleration factor function is related to the relationship between a testing time of the testing environment and a real time of a normal operating environment; performs~~. Next a simulating process that uses a testing time function is ~~used~~ performed to simulate the failure rate versus testing time relation~~; performs~~. Then a transforming process ~~by using~~ that uses the acceleration factor function is performed to transform the testing time function into a real time function~~, wherein a knee point of the real time function corresponds to an operation time which is the best burn in time;~~. ~~and performs~~ Finally, an integrating process is performed to integrate the real time function through a calculating region to ~~consult~~ acquire an accumulated failure rate real time function~~, wherein the calculating region is a region in which the real time is larger than the best burn in time~~. ~~Further, while more than one integrated circuits are failed before the knee point, the method further comprising deleting part of testing records and re calculating the best burn in time until only one integrated circuit is fail before the knee point~~.